

Claims

- [c1] A silicon-on-insulator integrated structure comprising:
at least one active region comprising active devices;
at least one bulk region adapted to provide structural support to said active region; and
at least one decoupling capacitor, wherein said decoupling capacitor includes capacitive fingers extending into said bulk region.
- [c2] The structure in claim 1, further comprising one or more common lower plates in said bulk region below said capacitive fingers of said decoupling capacitors.
- [c3] The structure in claim 1, wherein said capacitive fingers comprise one or more trenches lined with an insulator and filled with a conductor.
- [c4] The structure in claim 3, further comprising an upper plate connected to said conductor within said capacitive fingers.
- [c5] The structure in claim 4, wherein said upper plate extends from said decoupling capacitor into said active region.

- [c6] The structure in claim 1, further comprising a bulk contact adapted to bias said bulk region.
- [c7] The structure in claim 1, wherein said decoupling capacitor comprises a storage element of a dynamic random access memory (DRAM) memory element.
- [c8] A silicon-on-insulator integrated structure comprising:
 - at least one active region comprising active switching devices;
 - at least one bulk region adapted to provide structural support to said active region, said bulk region being devoid of active switching devices;
 - at least one decoupling capacitor, wherein said decoupling capacitor includes capacitive fingers extending vertically into said bulk region in a direction perpendicular to the horizontal upper surface of said bulk region.
- [c9] The structure in claim 8, further comprising a common lower plate in said bulk region below said capacitive fingers of said decoupling capacitors.
- [c10] The structure in claim 8, wherein said capacitive fingers comprise trenches lined with an insulator and filled with a conductor.
- [c11] The structure in claim 10, further comprising an upper plate connected to said conductor within said capacitive

fingers.

[c12] The structure in claim 11, wherein said upper plate extends from said decoupling capacitor into said active region.

[c13] The structure in claim 8, further comprising a bulk contact adapted to bias said bulk region.

[c14] The structure in claim 8, wherein said decoupling capacitor comprises a storage element of a dynamic random access memory (DRAM) memory element.

[c15] A method of forming a silicon-on-insulator integrated structure, said structure comprising at least one active region comprising active devices, and at least one bulk region adapted to provide structural support to said active region, said method comprising:
patterning finger openings into said bulk region;
lining said finger openings with an insulator; and
filling said finger openings with a conductor to form capacitive fingers extending into said bulk region.

[c16] The method in claim 15, further comprising, before said patterning of said finger openings, doping said bulk region to form a common lower plate in said bulk region below areas where said capacitive fingers will be formed.

- [c17] The method in claim 15, where said filling process simultaneously fills said finger openings, source and drain regions of transistors in said active region, bulk contacts in said bulk region, and plate contacts in said bulk region with said conductor.
- [c18] The method in claim 15, wherein said patterning, lining, and filling processes form different types of decoupling capacitors for different types of power supply designs.
- [c19] The method in claim 15, wherein said insulator is formed separately from gate insulators of transistors in said active area.
- [c20] The method in claim 15, further comprising connecting said decoupling capacitor to a transistor such that said decoupling capacitor comprises a storage element of a dynamic random access memory (DRAM) memory element.
- [c21] A method of forming a silicon-on-insulator integrated structure, said structure comprising at least one active region comprising active devices, and at least one bulk region adapted to provide structural support to said active region, said method comprising:
protecting said active region with a first mask;
depositing self-assembling nanoparticles on said bulk

region as a second mask;
patterning finger openings into said bulk region through said second mask;
lining said finger openings with an insulator; and
filling said finger openings with a conductor to form capacitive fingers extending into said bulk region.

[c22] The method in claim 21, further comprising, before said patterning of said finger openings, doping said bulk region to form a common lower plate in said bulk region below areas where said capacitive fingers will be formed.

[c23] The method in claim 21, where said filing process simultaneously fills said finger openings, source and drain regions of transistors in said active region, bulk contacts in said bulk region, and plate contacts in said bulk region with said conductor.

[c24] The method in claim 21, wherein said patterning, lining, and filling process form different types of decoupling capacitors for different types of power supply designs.

[c25] The method in claim 21, wherein said insulator is formed separately from gate insulators of transistors in said active area.

[c26] The method in claim 21, further comprising connecting said decoupling capacitor to a transistor such that said

decoupling capacitor comprises a storage element of a dynamic random access memory (DRAM) memory element.